

Loading Pe VCAL Data Calibrated on Mon Mar 10 18:30:06 2025 with release f7.29.4.1

Loading Dp VCAL Data Calibrated on Mon Mar 10 18:29:41 2025 with release f7.29.4.1

Site 1, Chassis 1, Slot 1, Slice 1

Board Name	PWB Number	PWB Rev	PWA Number	PWA Rev
HSB4DFE	521403	1	517352	14
PE256D	518540	4	519703	8
DP4FSER	522503	1	522282	3

Nextest Release: C:\nextest\f7.29.4.1

Test Program: Y:\nextest\f7.29.4.1\Bin\VernierCal_MagV.exe

Host Computer: FMNSGMAG5011

NOTE: Before hitting Start:

1. Close the ZIFs,
2. Turn DUT Board Power on,
3. Make sure no DSA is attached to the TIU.

The test program is loaded [C:\nextest\f7.29.4.1|a130e37|using map type NC].

TestStarted(1)...

Started: Mon Mar 10 18:37:11 2025

Starting Close ZIFs 1...

Info: test block tb_mag5_tiu_nvm_init has been bypassed, based on:

uv_bypass_tiu_nvm_init

Starting Mag5 CMLR and Clock 800 calibrations

CMLR Cal...

Clock 800 Cal...

Starting Mag5 EG Linearity calibration

Measuring drive linearity...

Measuring compare linearity...

Measuring wavetool linearity...

Starting Mag5 Analog Deskew calibration...

Measuring drive analog deskews...

Measuring compare analog deskews...

Measuring strobe analog deskews...

Starting Mag5 Edge to Edge measurements

testing odd mux pins

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testing even mux pins

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measuring wavetool strobes

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Starting TDR of PE round trip path...

Filling TDR NVM image header...

No Portable TDR Base measurements made, they are not performed for this configuration.

VernierCal_Magnum5: passed and the TCal file has been written.

Done: Mon Mar 10 18:48:14 2025

TestDone...bin = pass_bin,pass_bin

The test program is unloaded