

Test Program Y:\nextest\f7.29.4.1\Bin\SystemDiag.exe

Loading Pe VCAL Data Calibrated on Thu Feb 27 08:43:26 2025 with release f7.29.4.1

Loading Dp VCAL Data Calibrated on Thu Feb 27 08:43:01 2025 with release f7.29.4.1

SystemDiag Load TCal File

TCal: Slowest drive pin is a_19em, -4.6710 ns

TCal File Load Success, All Sections. Clk800 and EgLinRam to HW. Switch to pZeroOutDeskews state

Creating pattern set => PE32_ps_lvm01X

Creating pattern set => PE32_ps_lvmLHVZ

Creating pattern set => Logic_set

Creating pattern set => PE32_ps_ddr_set

Creating pattern set => PE32_ps_set

Creating pattern set => PE32_tg_set

Creating pattern set => default_set

The test program is loaded [C:\nextest\f7.29.4.1|a130e37|using map type NC].

Reading Configuration File, c:\nextest\config.ini:

HostName: FMNSGMAG5011

Nextest software release: c:\nextest\f7.29.4.1

TestStarted(1)...

Started: Mon Mar 10 18:01:18 2025

Collecting hardware information. This can take several seconds:

Collecting SPC data .

Collecting UCD data .

Collecting APB data .

Collecting RPT data .

Collecting UPT data .

Current Time is: Mon Mar 10 18:01:22 2025

- Site controller details -

Intel(R) Xeon(R) CPU E3-1275 v5 @ 3.60GHz, 15912MB total physical memory.

Windows Embedded Standard

7601.win7sp1_gdr.150202-1526

- Revision Codes for Boards -

*** Summary of board set for SA pn: 522408 rev: 7, Opt pn: 525419 ***

Site 2 (Chassis 1, Slot 1, Slice 2)

Board PWB PWA PWA Misc HSBEX RCM X Y D

Name Number Number Rev Number Rev GBits GBits MBits bits bits bits

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HSB4DFE 1 517352 14 64 (2) 0 (0) 64 (1) 24* 24* 36*

PE256D_1 4 519703 8

DP4FSER_1 1 522282 3

BIB 1 515732 2

APB 773457 519712 1 519710 6 Firmware Revision (DLP): 6.16.9 Firmware Revision (DLM): 1.8.1

SPC xxxxxx xxxxxx x xxxxxx x Firmware Revision (DLP): 7.4.13 Firmware Revision (DLM): 1.8.0

* NOTE: The ECR X, Y, D bits represent the maximum allowable configuration.

- Power Supply IDs -

Assy Assy

Num Rev

- UCD9090 Device Revs -

Device	Model	Rev	Date
HSB_UCD9090_56D	HSB4_56D	3	140827
HSB_UCD9090_59D	HSB4_59D	3	140827
PE1_UCD9090_56D	PE256_56D	8	140626
PE1_UCD9090_95D	PE256_95D	1	130403
PE1_UCD9090_107D	PE256_107D	1	130403
DP1_UCD9090_59D	DP4_59D	2	160323

- Pin Electronics IDs -

Chip Type	Chip Num	Chip ID
PE (PE8-1)	U17	1
PE (PE8-1)	U21	1
PE (PE8-1)	U25	1
PE (PE8-1)	U29	1

PE (PE8-1) U18 1

PE (PE8-1) U22 1

PE (PE8-1) U26 1

PE (PE8-1) U30 1

PE (PE8-1) U19 1

PE (PE8-1) U23 1

PE (PE8-1) U27 1

PE (PE8-1) U31 1

PE (PE8-1) U20 1

PE (PE8-1) U24 1

PE (PE8-1) U28 1

PE (PE8-1) U32 1

- Timing Generator IDs -

Chip Type	Chip Num	Chip ID
TG (Tango)	U49	4
TG (Tango)	U53	4
TG (Tango)	U57	4
TG (Tango)	U61	4
TG (Tango)	U50	4

TG (Tango)	U54	4
TG (Tango)	U58	4
TG (Tango)	U62	4
TG (Tango)	U51	4
TG (Tango)	U55	4
TG (Tango)	U59	4
TG (Tango)	U63	4
TG (Tango)	U52	4
TG (Tango)	U56	4
TG (Tango)	U60	4
TG (Tango)	U64	4

- DP Board device IDs -

Chip Type	Chip Num	Chip ID
DPS (AD5560)	U91	S4
DPS (AD5560)	U92	S4
DPS (AD5560)	U93	S4
DPS (AD5560)	U94	S4
DPS (AD5560)	U95	S4
DPS (AD5560)	U96	S4

DPS (AD5560) U97 S4

DPS (AD5560) U98 S4

DPS (AD5560) U99 S4

DPS (AD5560) U100 S4

DPS (AD5560) U101 S4

DPS (AD5560) U102 S4

DPS (AD5560) U103 S4

DPS (AD5560) U104 S4

DPS (AD5560) U105 S4

DPS (AD5560) U106 S4

DPS (AD5560) U123 S4

DPS (AD5560) U124 S4

DPS (AD5560) U125 S4

DPS (AD5560) U126 S4

DPS (AD5560) U127 S4

DPS (AD5560) U128 S4

DPS (AD5560) U129 S4

DPS (AD5560) U130 S4

DPS (AD5560) U131 S4

DPS (AD5560) U132 S4

DPS (AD5560) U133 S4

DPS (AD5560) U134 S4

DPS (AD5560) U135 S4

DPS (AD5560) U136 S4

DPS (AD5560) U137   S4

DPS (AD5560) U138   S4

- HSB Temperatures -

Device temp

HSB_AIR_IN = 29

HSB_AIR_OUT = 24

HSB_EX1_SNSR = 37

HSB_EX1_DIODE = 47

HSB_EX2_SNSR = 34

HSB_EX2_DIODE = 42

HSB_CPUI_SNSR = 33

HSB_CPUI_DIODE = 40

- PE Temperatures -

Device = temp Device = temp Device = temp Device = temp

SL2_PE1 = 62 SL2_PE2 = 62 SL2_PE3 = 62 SL2_PE4 = 61

SL2_PE5 = 61 SL2_PE6 = 62 SL2_PE7 = 61 SL2_PE8 = 62

SL2_PE9 = 62 SL2_PE10 = 64 SL2_PE11 = 62 SL2_PE12 = 61

SL2_PE13 = 60 SL2_PE14 = 60 SL2_PE15 = 59 SL2_PE16 = 59

Device = temp Device = temp Device = temp Device = temp

SL2_TANGO1 = 56 SL2_TANGO2 = 55 SL2_TANGO3 = 54 SL2_TANGO4 = 53

SL2_TANGO5 = 53 SL2_TANGO6 = 53 SL2_TANGO7 = 49 SL2_TANGO8 = 53

SL2_TANGO9 = 59 SL2_TANGO10 = 52 SL2_TANGO11 = 52 SL2_TANGO12 = 50

SL2_TANGO13 = 51 SL2_TANGO14 = 50 SL2_TANGO15 = 50 SL2_TANGO16 = 50

Device temp

LIQ_IN = 45

LIQ_OUT = 35

AIR_BOTCTR = 50

AIR_LO = 33

AIR_HI = 32

PG1_SNSR = 32

PG1_DIODE = 34

PG2_SNSR = 32

PG2_DIODE = 34

- DP Temperatures -

Device = temp Device = temp Device = temp Device = temp

SL2_DPSA1 = 31 SL2_DPSA1X = 31 SL2_DPSA2 = 32 SL2_DPSA2X = 32

SL2_DPSA3 = 32 SL2_DPSA3X = 31 SL2_DPSA4 = 30 SL2_DPSA4X = 31

SL2_DPSA5 = 31 SL2_DPSA5X = 31 SL2_DPSA6 = 31 SL2_DPSA6X = 32

SL2_DPSA7 = 31 SL2_DPSA7X = 31 SL2_DPSA8 = 30 SL2_DPSA8X = 31

SL2_DPSB1 = 32 SL2_DPSB1X = 32 SL2_DPSB2 = 32 SL2_DPSB2X = 33

SL2_DPSB3 = 32 SL2_DPSB3X = 32 SL2_DPSB4 = 31 SL2_DPSB4X = 32

SL2_DPSB5 = 31 SL2_DPSB5X = 31 SL2_DPSB6 = 31 SL2_DPSB6X = 31

SL2_DPSB7 = 31 SL2_DPSB7X = 31 SL2_DPSB8 = 30 SL2_DPSB8X = 31

Device temp

AIR_TOPCTR = 29

AIR_ADT7461 = 30

- HSB Voltages -

Device = Volts Device = Volts Device = Volts Device = Volts

V0P75 = 0.751 V0P85_CPUI = 0.852 V1P0 = 1.002 V1P5 = 1.505

V1P5_DIMM_G1 = 1.606 V1P5_DIMM_G2 = 1.609 V3P3 = 3.314 V2P5_EX1 = 2.503

V2P5_EX2 = 2.493 V2P5_CPUI = 2.499 V3P3_CTRL = 3.309 V5P_CTRL = 5.021

V5P_CTRL_SB = 5.000 V5P_AUX = 5.174 V12P_CTRL = 12.005 V3P0_EX1 = 2.996

V3P0_EX2 = 2.999 V3P0_CPUI = 2.998 V0P9_EX1 = 0.902 V0P9_EX2 = 0.901

SPC_AGND = -0.001 V4P096_REF = 4.097 V12P_HSB = 11.983 V12P_HSK = 11.938

V12P_AUX = 11.958 V12P_SPC_OR = 11.672 SPC_V5P = 5.042 SPC_V5PF = 6.023

SPC_V4P_RAW = 3.800 SPC_V4P = 3.782 SPC_V16P5 = 16.508 SPC_V8M5 = -8.529

IPS_ISHARE = 1.208 V3P3_UCD = 3.303 V3P3_CTRL_SB = 3.284

- PE Voltages -

Device = Volts Device = Volts Device = Volts Device = Volts

V7P6_SL1 = 7.602 V7P6_SL2 = 7.599 V4M35_SL1 = -4.350 V4M35_SL2 = -4.349

V1P15_SL1-1 = 1.313 V1P15_SL1-2 = 1.311 V1P15_SL2-1 = 1.312 V1P15_SL2-2 = 1.313

V1P2A_SL1 = 1.201 V1P2A_SL2 = 1.202 V0P85_SL1 = 0.900 V0P85_SL2 = 0.901

V0P75_TG = 0.749 V0P75 = 0.748 V1P5_TG = 1.502 V1P5_SL1 = 1.500

V1P5_SL2 = 1.499 V1P8 = 1.806 V2P5_PE = 2.500 V2P5 = 2.503

V3P3 = 3.304 V3P0 = 3.002 V11P5 = 11.518 V17P5 = 17.464

V1P0_SL1 = 0.999 V1P0_SL2 = 0.996 SPC_V3P3 = 3.268

- DP Voltages -

Device = Volts Device = Volts Device = Volts Device = Volts

V7M75 = -10.011 V4M5 = -4.506 V1P2 = 1.200 V1P5 = 1.497

V2P5 = 2.501 V3P3 = 3.296 V15P0 = 16.751 V32P0 = 31.977

- Revision Codes for Memory Modules -

Module Name	DIMM Function	Base Number	PGM Number	PGM Rev	Misc GBits	RCM MBits	HSBEX GBits
PE1-DIMM-1 (J16)	ECR (0x3)	516726	519245	1		32	
PE1-DIMM-2 (J17)	ECR (0x3)	516726	519245	1		32	
PE1-RCM (J13)		514846	519637	3		64	

- Vendor Information for Standard DIMM Memory Modules -

Module Name	Dimm Vendor	Dimm Vendor Rev	Dimm Date	Dimm Dram Vendor	Dimm Dram Rev
PE1-DIMM-1 (J16)	N/A	WD3CE84G16NISF-NXT	1 1720	N/A	N/A
PE1-DIMM-2 (J17)	N/A	WD3CE84G16NISF-NXT	1		

1720 N/A N/A

PE1-RCM (J13) NEXTEST 3 N/A N/A N/A

- Revision Codes for FPGAs -

FPGA Name	SW Rev	HW Rev
CPUI Fpga	0x1	0x15
HD4 PG Fpga	0x2	0xd
HD4 PG Fpga	0x2	0xd
HD4 PG Fpga	0x2	0xd
HD4 PG Fpga	0x2	0xd
HD4 DP Fpga	0x1	0x21
HD4 DP Fpga	0x1	0x21
HD4 DP Fpga	0x1	0x21
HD4 DP Fpga	0x1	0x21
HD4 ECR-EX FPGA	0x1	0x12
HD4 ECR-EX FPGA	0x1	0x12
HD4 ECR-EX FPGA	0x1	0x12
HD4 ECR-EX FPGA	0x1	0x12

Nextest software release: C:\nextest\f7.29.4.1\Bin\Ui.exe

Running on MagnumV_EV_System system# 900282

HOST computer name: fmnsgmag5011

PCC = 116

PRC = 0

Delta = 116

Calibration Time and Environment :-

Cal Cal Host Software Cal Hsb Ipc Dp Dp Pe Pe

Module Chas/Slot/Mod Date Time Name Relase

DP_1 1 1 1 Thu Feb 27 08:43:01 2025 FMNSGMAG5011

PE_1 1 1 1 Thu Feb 27 08:43:26 2025 FMNSGMAG5011 f7.29.4.1

Testing for proper PCIe configuration [check_pcie_config_tb]

Testing CPUI to PG Bus [cpui_pg_busdiag_tb]

Testing APG read,write registers via cpu [apg_rw_regs_tb]

  Testing Address registers and LBDATA

  Testing JAM, DMAIN, DBASE, YINDEX

  Testing Unique values

Testing PG to TG Bus [pg_tg_busdiag_tb]

  PG_TG Bus Test phase 1a Low Speed: PG register 64-Bit I/O...

  PG_TG Bus Test phase 2a Low Speed: Bit Independence...

  PG_TG Bus Test phase 3a Low Speed: Marching (1)...

  PG_TG Bus Test phase 4a Low Speed: Marching (0)...

  PG_TG Bus Test phase 5a Low Speed: Tango Device Independence

  PG_TG Bus Test phase 6a Low Speed: Tango Broadcast Mode

  PG_TG Bus Test phase 1b High Speed: PG register 64-Bit I/O...

  PG_TG Bus Test phase 2b High Speed: Bit Independence...

  PG_TG Bus Test phase 3b High Speed: Marching (1)...

  PG_TG Bus Test phase 4b High Speed: Marching (0)...

  PG_TG Bus Test phase 5b High Speed: Tango Device Independence

  PG_TG Bus Test phase 6b High Speed: Tango Broadcast Mode

Calibrating TG CMLR and Clock 800 [tg_clk800_cal_tb]

  Vernier Cal Loaded

  Skip tg_clk800_cal_tb: clk800 cal Data already loaded

Testing TG Device [tg_pik_ram_tb]

  TG Pik Ram Test Phase 1

Datum 00000055

Datum 000000AA

Datum 000000FF

Datum 00000000

TG Pik Ram Test Phase 2

Testing TG Device [tg_edgeset_ram_tb]

TG EdgeSet RAM Test Phase 1

TG EdgeSet RAM Test Phase 2

Testing TG Device [tg_compare_fifo_tb]

TG Compare A/B Fifo RAM Test Phase 1

TG Compare A/B Fifo RAM Test Phase 2

Testing TG Device [tg_lin_ram_tb]

TG Linearity RAM Test Phase 1

TG Linearity RAM Test Phase 2

Testing TG Device [tg_tgmap_ram_tb]

TG Map RAM Test Phase 1

TG Map Ram Test Phase 2

Testing TG Device [tg_tgmap_ka_ram_tb]

TG Map KA RAM Test Phase 1

TG Map KA Ram Test Phase 2

Testing TG Device [tg_common_fifos_tb]

TG Common Fifo RAM Test phase 1:

TG Common Fifo RAM Test phase 2:

TG Common Fifo RAM Test phase 3:

TG Common Fifo RAM Test phase 4:

Testing TG Device [tg_period_mem_tb]

TG Period Memory Test Phase 1

Datum 05555555

Datum 02AAAAAA

Datum 07FFFFFF

Datum 00000000

TG Period Memory Test Phase 2

Testing TG Device [tg_wt_match_fifo_tb]

TG Wavetool Match Fifo RAM Test Phase 1

TG Wavetool Match Fifo RAM Test Phase 2

Testing TG Device [tg_wt_lin_ram_tb]

TG Wavetool Linear Calibration RAM Test Phase 1

TG Wavetool Linear Calibration RAM Test Phase 2

Testing TG Device [tg_wt_capture_ram_tb]

TG Wavetool Capture RAM Test Phase 1

TG Wavetool Capture RAM Test Phase 2

Testing PG Error Counter [pg_err_cntr_tb]

Testing TG Device [tg_siggen_ecr_tb]

TG ECR Bus Signature Analysis Test Phase 2: Full Bus

Testing TG Device [tg_siggen_pg_tb]

TG PG Bus Signature Analysis Test Phase 1: Static Vector

TG PG Bus Signature Analysis Test Phase 2: Lfsr PRBS Stream Full bus

Testing TG Period Generator [tg_period_gen_tb]

Test Tango Period Generator and Residue Fanout. Table Loops = 4000

Pattern Duration = 538076 clock cycles

TG Edge Signature Analyzer Test [tg_siggen_edge_tb]

Test digital section of EdgeFireBus, Period Generator, TG Drive Circuitry, and APG

Testing TG ECR Cross Point [tg_ecr_xpoint_tb]

TG ECR Cross Point Test Phase 1: Full 32-bit bus Pass-Through Mode 1M Vectors: Previous

TG ECR Cross Point Test Phase 2 on column 1: SingleBit Previous Multiplexing

TG ECR Cross Point Test Phase 3 on column 2: SingleBit Previous Multiplexing

TG ECR Cross Point Test Phase 4 on column 3: SingleBit Previous Multiplexing

TG ECR Cross Point Test Phase 5: Full 32-bit bus Pass-Through Mode: Local Strobe

Test: Drive High No Strobe 0x00

Test: Strobe Pass Window 0x00

Test: Strobe Open Window 0x01

Test: Strobe Open Window 0x02

Test: Strobe Open Window 0x03

Test: Strobe Close Window 0x01

Test: Strobe Close Window 0x02

Test: Strobe Window Glitch 0x01

Test: Pass_DDR_SuperMux 0x00

Test: A_DDR_SuperMux 0x04

Test: B_DDR_SuperMux 0x08

TG ECR Cross Point Test Phase 6 on column (cpu_id) 0: Local Strobe Single Bit Multiplexing

TG ECR Cross Point Test Phase 7 on column (cpu_id) 1: Local Strobe Single Bit Multiplexing

TG ECR Cross Point Test Phase 8 on column (cpu_id) 2: Local Strobe Single Bit Multiplexing

TG ECR Cross Point Test Phase 9 on column (cpu_id) 3: Local Strobe Single Bit Multiplexing

Testing PG to Tango DMA [pg_tg_dma_tb]

PG TG Dma Test Phase 1: General dma block I/O

PG TG Dma Test Phase 2: Vary Dma Block Size

Testing TG WaveTool [tg_wt_tb]

do_wt_deskew_calibrate(): Start

Pass 0 using CH0

Pass 1 using CH1

do_wt_deskew_calibrate(): End: 64 seconds

WT Deskew Calibration SUCCESS

TG WaveTool Test Phase 0: Test 0 BL CH0

TG WaveTool Test Phase 1: Test 1 AH CH0

TG WaveTool Test Phase 2: Test 2 BL CH0 major residue

TG WaveTool Test Phase 3: Test 3 BL CH0, WT all zero

TG WaveTool Test Phase 4: Test 4 BL CH0, WT all one

TG WaveTool Test Phase 5: Test 5 BL CH1, WT all one

TG WaveTool Test Phase 6: Test 6 AH CH0

TG WaveTool Test Phase 7: Test 7 AH CH1

TG WaveTool Test Phase 8: Test 8 BL CH1

TG Dut Error Flag Test [tg_dut_error_flag_tb]

Testing NOLATCH Case (RECORD is FALSE)

Testing LATCH Case (RECORD is TRUE)

PG TG Pattern Basic Timing Test 1 [pg_tg_cyc_nores__edges_within_cyc_tb]

PG TG Pattern Basic Timing Test 2
[pg_tg_cyc_nores__edges_on_clks_nores_tb]

PG TG Pattern Basic Timing Test 3
[pg_tg_cyc_nores__edges_on_clks_res_tb]

PG TG Pattern Basic Timing Test 4 [pg_tg_cyc_res__edges_at_0_nores_tb]

PG TG Pattern Basic Timing Test 5
[pg_tg_cyc_res__edges_on_clks_nores_tb]

PG TG Pattern Basic Timing Test 6 [pg_tg_cyc_res__edges_on_clks_res_tb]

PG TG Pattern Basic Timing Test 7
[pg_tg_cyc_roll_over__edges_at_0_nores_tb]

PG TG Pattern Basic Timing Test 8
[pg_tg_cyc_roll_over__edges_on_clks_nores_tb]

PG TG Pattern Basic Timing Test 9
[pg_tg_cyc_roll_over__edges_on_clks_res_tb]

Testing PG comm to adjacent slice [pg_slice_reg_tb]

Testing PE error generation [pe_error_gen_tb]

Testing PE force drive state [pe_force_drive_state_tb]

Testing PE force drive state [pe_vz_state_tb]

Testing strobe modes [pe_strobe_mode_tb]

Test Edge and Window modes single data rate mode

Test A and B cycle PES functions in dual data mode

Tango Channel Parking Test [tg_parking_tb]

Test CPU Parking

Test DE Parking

Test DD Parking

Test Pattern Drive/Strobe Parking

Testing DP ADC [adc_tb]

Verify Adc Input 1 (Default Measure Path)

Verify Adc Input 2 (HCVdd_1 - Tracking Supply)

Verify Adc Input 3 (HCVdd_2 - Tracking Supply)

Verify Adc Input 4 (VREF_V1P17 - ADC Offset Voltage)

Testing ADC Capture Ram memory march [adc_capture_ram_march_tb]

Performing walking ones test on data bus.

Performing walking ones test on address bus.

Testing DP PMU voltage force [pmu_vf_tb]

Testing DP 1 PMU voltage force level accuracy

Testing DP PMU current force [pmu_if_tb]

Testing DP 1 PMU current force level accuracy

Testing DP PMU current measure capability [pmu_imeas_tb]

Testing DP1

Testing PMU range 1 (5 uA)

Testing PMU range 2 (20 uA)

Testing PMU range 3 (200 uA)

Testing PMU range 4 (2 mA)

Testing PMU range 5 (20 mA)

Testing DP PMU common mode [pmu_cmode_tb]

Testing DP1 PMU range 1 (5 uA)

Testing DP1 PMU range 2 (20 uA)

Testing DP1 PMU range 3 (200 uA)

Testing DP1 PMU range 4 (2 mA)

Testing DP1 PMU range 5 (20 mA)

Testing DP PMU voltage clamps [pmu_vclamp_tb]

Testing DP PMU current limit [pmu_ilimit_tb]

Testing DPS voltage tracking [dps_vtrack_tb]

Testing DPS tracking supplies (Ascending)

Testing DPS tracking supplies (Descending)

Testing DPS voltage force [dps_vf_tb]

Testing DP DPS pin level DACs

Testing DP DPS pin level accuracy

Testing DP DPS pin level accuracy (High Current)

Testing DP DPS pin level accuracy voltage -7 to -3 and 11 to 13

Testing DPS switches [dps_switch_tb]

Testing DPS Switch "all open"

Testing DPS Switch "all closed"

Testing DPS Switch "DPS_F open"

Testing DPS Switch "DPS sys_force/sense open"

Testing DPS Switch "DPS local feedback"

Testing DPS current measure [dps_imeas_tb]

Testing DPS current share [dps_ishare_tb]

Testing DPS current share in x2 mode (No X pins)

Testing by x2 'a' pins with DPS range 1

Testing by x2 'a' pins with DPS range 2

Testing by x2 'a' pins with DPS range 3

Testing by x2 'a' pins with DPS range 4

Testing by x2 'a' pins with DPS range 5

Testing by x2 'a' pins with DPS range 6

Testing by x2 'a' pins with DPS range 7

Testing DPS current share in x4 mode (No X pins)

Testing by x4 'a' pins with DPS range 1

Testing by x4 'a' pins with DPS range 2

Testing by x4 'a' pins with DPS range 3

Testing by x4 'a' pins with DPS range 4

Testing by x4 'a' pins with DPS range 5

Testing by x4 'a' pins with DPS range 6

Testing by x4 'a' pins with DPS range 7

Testing DPS current share in x8 mode (No X pins)

Testing by x8 'a' pins with DPS range 1

Testing by x8 'a' pins with DPS range 2

Testing by x8 'a' pins with DPS range 3

Testing by x8 'a' pins with DPS range 4

Testing by x8 'a' pins with DPS range 5

Testing by x8 'a' pins with DPS range 6

Testing by x8 'a' pins with DPS range 7

Testing DPS current share in x2 mode (Using X pins)

Testing by x2 'a' pins with DPS range 1

Testing by x2 'a' pins with DPS range 2

Testing by x2 'a' pins with DPS range 3

Testing by x2 'a' pins with DPS range 4

Testing by x2 'a' pins with DPS range 5

Testing by x2 'a' pins with DPS range 6

Testing by x2 'a' pins with DPS range 7

Testing by x2 'b' pins with DPS range 1

Testing by x2 'b' pins with DPS range 2

Testing by x2 'b' pins with DPS range 3

Testing by x2 'b' pins with DPS range 4

Testing by x2 'b' pins with DPS range 5

Testing by x2 'b' pins with DPS range 6

Testing by x2 'b' pins with DPS range 7

Testing DPS current share in x4 mode (Using X pins)

Testing by x4 'a' pins with DPS range 1

Testing by x4 'a' pins with DPS range 2

Testing by x4 'a' pins with DPS range 3

Testing by x4 'a' pins with DPS range 4

Testing by x4 'a' pins with DPS range 5

Testing by x4 'a' pins with DPS range 6

Testing by x4 'a' pins with DPS range 7

Testing DPS current share in x8 mode (Using X pins)

Testing by x8 'a' pins with DPS range 1

Testing by x8 'a' pins with DPS range 2

Testing by x8 'a' pins with DPS range 3

Testing by x8 'a' pins with DPS range 4

Testing by x8 'a' pins with DPS range 5

Testing by x8 'a' pins with DPS range 6

Testing by x8 'a' pins with DPS range 7

Testing DPS current share in x16 mode (Using X pins)

Testing by x16 'a' pins with DPS range 1

Testing by x16 'a' pins with DPS range 2

Testing by x16 'a' pins with DPS range 3

Testing by x16 'a' pins with DPS range 4

Testing by x16 'a' pins with DPS range 5

Testing by x16 'a' pins with DPS range 6

Testing by x16 'a' pins with DPS range 7

Testing DPS leakage current [dps_leakage_tb]

Testing DPS Leakage with PMU IMeas

Testing DPS Leakage with DPS IMeas

Testing DP HV voltage force [hv_vf_tb]

Testing HV DACs

Testing HV level accuracy

Testing DP HV apg level DAC select path

Testing DP HV current measure [hv_imeas_tb]

HV I Measure @ Range1 (12 mA)

Testing @ -2.500V

Testing @ 5.500V

Testing @ 13.500V

Testing @ 21.500V

Testing @ 29.500V

Testing DP HV leakage current [hv_leakage_tb]

Testing PE leakage current [pe_leakage_tb]

Testing PMU Leakage with PMU VForce

Testing PE Leakage with PMU VForce

Testing PE VIH pin level [vih_tb]

Testing VIH level accuracy

Testing VIH apg level DAC select path

Testing PE VIL pin level [vil_tb]

Testing VIL level accuracy

Testing VIL apg level DAC select path

Testing PE VIHH pin level [vihh_tb]

Testing VIHH level accuracy

Testing PE VTT pin level [vtt_tb]

Testing PE VOH pin level [voh_tb]

Testing PE VOL pin level [vol_tb]

Testing PE VZ pin level [vz_tb]

Testing PE IOH pin level [ioh_tb]

Testing IOH level accuracy

Testing PE IOL pin level [iol_tb]

Testing IOL level accuracy

Testing PE Reflection Voltage Clamps [ref_clamps_tb]

Testing Reflection Clamp LOW

Testing Reflection Clamp HIGH

Testing PE output impedance [pe_rout_tb]

Testing PE Cable Compensation [pe_cable_comp_tb]

Switch to Calibrated Deskews and Lin Ram

Switch to pZeroOutDeskews

Testing PE XYZ Address SDR Pin Scramble [pe_ps_xyz_tb]

Testing X Address bits

X Address 50.0MHz Test (20 ns)

Testing Y Address bits

Y Address 50.0MHz Test (20 ns)

Testing Z Address bits

Z Address 50.0MHz Test (20 ns)

Testing PE Data Pin Scramble [pe_ps_data_tb]

Testing Data bits

Data Bits 50.0MHz Test (20 ns)

Testing Data Strobes

Data Strobes 20.0MHz Test (50 ns)

Testing PE Chip Select Pin Scramble [pe_ps_cs_tb]

Testing Chip Selects

Chip Selects 50.0MHz Test (20 ns)

Testing Chip Select Strobes

Chip Select Strobes 4.0MHz Test (250 ns)

Testing PE Force Pin Scramble [pe_ps_force_tb]

Testing Drive L/H/Z

Drive Low 50.0MHz Test (20 ns)

Drive High 50.0MHz Test (20 ns)

Tri-State 50.0MHz Test (20 ns)

Testing Strobe L/H/V/M

Strobe Low 20.0MHz Test (50 ns)

Strobe High 20.0MHz Test (50 ns)

Strobe Valid 20.0MHz Test (50 ns)

Strobe Mid 20.0MHz Test (50 ns)

Testing PE XYZ Address DDR Pin Scramble [pe_ps_xyz_ddr_tb]

Testing X Address bits

X Address 50.0MHz Test (20 ns)

Testing Y Address bits

Y Address 50.0MHz Test (20 ns)

Testing Z Address bits

Z Address 50.0MHz Test (20 ns)

Testing PE Data Pin Scramble [pe_ps_data_ddr_tb]

Testing Data bits

Data Bits 50.0MHz Test (20 ns)

Testing Data Strobes

Data Strobes 20.0MHz Test (50 ns)

Testing PE Chip Select Pin Scramble [pe_ps_cs_ddr_tb]

  Testing Chip Selects

    Chip Selects 50.0MHz Test (20 ns)

  Testing Chip Select Strobes

    Chip Select Strobes 4.0MHz Test (250 ns)

Testing PE Force Pin Scramble [pe_ps_force_ddr_tb]

  Testing Drive L/H/Z

    Drive Low 50.0MHz Test (20 ns)

    Drive High 50.0MHz Test (20 ns)

    Tri-State 50.0MHz Test (20 ns)

  Testing Strobe L/H/V/M

    Strobe Low   20.0MHz Test (50 ns)

    Strobe High 20.0MHz Test (50 ns)

Testing TG->PE Timing Formats [pe_tg_format_tb]

  Switch to Calibrated Deskews and Lin Ram

  Switch to pZeroOutDeskews

  Testing NRZ Format 5.0MHz Test (200 ns) with Edge Strobes

  Testing NRZ Format 5.0MHz Test (200 ns) with Window Strobes

  Testing RTO Format 5.0MHz Test (200 ns) with Edge Strobes

  Testing RTO Format 5.0MHz Test (200 ns) with Window Strobes

  Testing RTZ Format 5.0MHz Test (200 ns) with Edge Strobes

  Testing RTZ Format 5.0MHz Test (200 ns) with Window Strobes

  Testing RTC Format 5.0MHz Test (200 ns) with Edge Strobes

  Testing RTC Format 5.0MHz Test (200 ns) with Window Strobes

Testing SBC Format 5.0MHz Test (200 ns) with Edge Strobes

Testing SBC Format 5.0MHz Test (200 ns) with Window Strobes

Testing TG->PE Timing Generators [pe_tg_dclk_format_tb]

Switch to Calibrated Deskews and Lin Ram

Switch to pZeroOutDeskews

DCLKPOS Format 5.0MHz Test (cycle 200 ns, edge spacing 40.0 ns) Edge Strobes

DCLKPOS Format 5.0MHz Test (cycle 200 ns, edge spacing 40.0 ns) Window Strobes

DCLKNEG Format 5.0MHz Test (cycle 200 ns, edge spacing 40.0 ns) Edge Strobes

DCLKNEG Format 5.0MHz Test (cycle 200 ns, edge spacing 40.0 ns) Window Strobes

Testing TG->PE Timing Generators [pe_tg_mux_mode_tb]

Switch to Calibrated Deskews and Lin Ram

Switch to pZeroOutDeskews

Testing MUX Mode 5.0MHz Test (200 ns) with Edge Strobes

Testing MUX Mode 5.0MHz Test (200 ns) with Window Strobes

Testing DBM read widths at minimum speed configuration [dbm1_tb]

32-bit width data - 24X, 7Y, Seq_Length 1 (pass1, loop1)

16-bit width data - 24X, 8Y, Seq_Length 1 (pass1, loop2)

8-bit width data - 24X, 9Y, Seq_Length 1 (pass1, loop3)

4-bit width data - 24X, 10Y, Seq_Length 1 (pass1, loop4)

2-bit width data - 24X, 11Y, Seq_Length 1 (pass1, loop5)

1-bit width data - 24X, 12Y, Seq_Length 1 (pass1, loop6)

32-bit width data - 7X, 24Y, Seq_Length 1 (pass2, loop1)

16-bit width data - 8X, 24Y, Seq_Length 1 (pass2, loop2)

8-bit width data - 9X, 24Y, Seq_Length 1 (pass2, loop3)

4-bit width data - 10X, 24Y, Seq_Length 1 (pass2, loop4)

2-bit width data - 11X, 24Y, Seq_Length 1 (pass2, loop5)

1-bit width data - 12X, 24Y, Seq_Length 1 (pass2, loop6)

Testing DBM read speed with 32-bit data [dbm2_tb]

17 X, 14 Y at   2.5000ns, Seq_Length 64, (pass1, loop1)

17 X, 13 Y at   2.5000ns, Seq_Length 32, (pass1, loop2)

17 X, 14 Y at   3.3334ns, Seq_Length 32, (pass1, loop3)

17 X, 12 Y at   2.5000ns, Seq_Length 16, (pass1, loop4)

17 X, 13 Y at   3.3334ns, Seq_Length 16, (pass1, loop5)

17 X, 14 Y at   6.6667ns, Seq_Length 16, (pass1, loop6)

17 X, 11 Y at   2.5000ns, Seq_Length 8, (pass1, loop7)

17 X, 12 Y at   3.3334ns, Seq_Length 8, (pass1, loop8)

17 X, 13 Y at   6.6667ns, Seq_Length 8, (pass1, loop9)

17 X, 14 Y at 13.3334ns, Seq_Length 8, (pass1, loop10)

17 X, 10 Y at   2.5000ns, Seq_Length 4, (pass1, loop11)

17 X, 11 Y at   3.3334ns, Seq_Length 4, (pass1, loop12)

17 X, 12 Y at   6.6667ns, Seq_Length 4, (pass1, loop13)

17 X, 13 Y at 13.3334ns, Seq_Length 4, (pass1, loop14)

17 X, 14 Y at 26.5958ns, Seq_Length 4, (pass1, loop15)

17 X, 9 Y at   2.5000ns, Seq_Length 2, (pass1, loop16)

17 X, 10 Y at   3.3334ns, Seq_Length 2, (pass1, loop17)

17 X, 11 Y at 6.6667ns, Seq_Length 2, (pass1, loop18)

17 X, 12 Y at 13.3334ns, Seq_Length 2, (pass1, loop19)

17 X, 13 Y at 26.5958ns, Seq_Length 2, (pass1, loop20)

17 X, 14 Y at 53.1915ns, Seq_Length 2, (pass1, loop21)

17 X, 9 Y at 3.3334ns, Seq_Length 1, (pass1, loop22)

17 X, 10 Y at 6.6667ns, Seq_Length 1, (pass1, loop23)

17 X, 11 Y at 13.3334ns, Seq_Length 1, (pass1, loop24)

17 X, 12 Y at 26.5958ns, Seq_Length 1, (pass1, loop25)

17 X, 13 Y at 53.1915ns, Seq_Length 1, (pass1, loop26)

17 X, 14 Y at 106.3830ns, Seq_Length 1, (pass1, loop27)

17 X, 8 Y at 2.5000ns, Seq_Length 1, (pass1, loop28)

14 X, 17 Y at 2.5000ns, Seq_Length 64, (pass2, loop1)

13 X, 17 Y at 2.5000ns, Seq_Length 32, (pass2, loop2)

14 X, 17 Y at 3.3334ns, Seq_Length 32, (pass2, loop3)

12 X, 17 Y at 2.5000ns, Seq_Length 16, (pass2, loop4)

13 X, 17 Y at 3.3334ns, Seq_Length 16, (pass2, loop5)

14 X, 17 Y at 6.6667ns, Seq_Length 16, (pass2, loop6)

11 X, 17 Y at 2.5000ns, Seq_Length 8, (pass2, loop7)

12 X, 17 Y at 3.3334ns, Seq_Length 8, (pass2, loop8)

13 X, 17 Y at 6.6667ns, Seq_Length 8, (pass2, loop9)

14 X, 17 Y at 13.3334ns, Seq_Length 8, (pass2, loop10)

10 X, 17 Y at 2.5000ns, Seq_Length 4, (pass2, loop11)

11 X, 17 Y at 3.3334ns, Seq_Length 4, (pass2, loop12)

12 X, 17 Y at 6.6667ns, Seq_Length 4, (pass2, loop13)

13 X, 17 Y at 13.3334ns, Seq_Length 4, (pass2, loop14)

14 X, 17 Y at 26.5958ns, Seq_Length 4, (pass2, loop15)

9 X, 17 Y at 2.5000ns, Seq_Length 2, (pass2, loop16)

10 X, 17 Y at 3.3334ns, Seq_Length 2, (pass2, loop17)

11 X, 17 Y at 6.6667ns, Seq_Length 2, (pass2, loop18)

12 X, 17 Y at 13.3334ns, Seq_Length 2, (pass2, loop19)

13 X, 17 Y at 26.5958ns, Seq_Length 2, (pass2, loop20)

14 X, 17 Y at 53.1915ns, Seq_Length 2, (pass2, loop21)

9 X, 17 Y at 3.3334ns, Seq_Length 1, (pass2, loop22)

10 X, 17 Y at 6.6667ns, Seq_Length 1, (pass2, loop23)

11 X, 17 Y at 13.3334ns, Seq_Length 1, (pass2, loop24)

12 X, 17 Y at 26.5958ns, Seq_Length 1, (pass2, loop25)

13 X, 17 Y at 53.1915ns, Seq_Length 1, (pass2, loop26)

14 X, 17 Y at 106.3830ns, Seq_Length 1, (pass2, loop27)

8 X, 17 Y at 2.5000ns, Seq_Length 1, (pass2, loop28)

Testing DBM write widths at minimum speed configuration [dbm3_tb]

32-bit width data - 24X, 7Y, Seq_Length 1 (pass1, loop1)

16-bit width data - 24X, 8Y, Seq_Length 1 (pass1, loop2)

8-bit width data - 24X, 9Y, Seq_Length 1 (pass1, loop3)

4-bit width data - 24X, 10Y, Seq_Length 1 (pass1, loop4)

2-bit width data - 24X, 11Y, Seq_Length 1 (pass1, loop5)

1-bit width data - 24X, 12Y, Seq_Length 1 (pass1, loop6)

32-bit width data - 7X, 24Y, Seq_Length 1 (pass2, loop1)

16-bit width data - 8X, 24Y, Seq_Length 1 (pass2, loop2)

8-bit width data - 9X, 24Y, Seq_Length 1 (pass2, loop3)

4-bit width data - 10X, 24Y, Seq_Length 1 (pass2, loop4)

2-bit width data - 11X, 24Y, Seq_Length 1 (pass2, loop5)

1-bit width data - 12X, 24Y, Seq_Length 1 (pass2, loop6)

Testing DBM write speed with 32-bit data [dbm4_tb]

16 X, 10 Y at 3.3334ns, Seq_Length 1, (pass1, loop1)

16 X, 11 Y at 6.6667ns, Seq_Length 1, (pass1, loop2)

16 X, 12 Y at 13.3334ns, Seq_Length 1, (pass1, loop3)

16 X, 13 Y at 26.5958ns, Seq_Length 1, (pass1, loop4)

16 X, 14 Y at 53.1915ns, Seq_Length 1, (pass1, loop5)

16 X, 15 Y at 106.3830ns, Seq_Length 1, (pass1, loop6)

16 X, 9 Y at 2.5000ns, Seq_Length 1, (pass1, loop7)

10 X, 16 Y at 3.3334ns, Seq_Length 1, (pass2, loop1)

11 X, 16 Y at 6.6667ns, Seq_Length 1, (pass2, loop2)

12 X, 16 Y at 13.3334ns, Seq_Length 1, (pass2, loop3)

13 X, 16 Y at 26.5958ns, Seq_Length 1, (pass2, loop4)

14 X, 16 Y at 53.1915ns, Seq_Length 1, (pass2, loop5)

15 X, 16 Y at 106.3830ns, Seq_Length 1, (pass2, loop6)

9 X, 16 Y at 2.5000ns, Seq_Length 1, (pass2, loop7)

SystemDiag summary [diag_summary_tb]

Pass number : 1

Time for this pass : 00:20:43

Total time : 00:20:49

Final Bin: pass_bin

Done: Mon Mar 10 18:22:01 2025

TestDone...bin =
pass_bin,pass_bin,pass_bin,pass_bin,pass_bin,pass_bin,pass_bin,pass_bin

The test program is unloaded